Institute of Electrical and Electronics Engineers

Hyderabad Section

Joint Chapter of MTT/AP/EMC Societies in Association with Joint Chapter of CAS/ED Societies Presents

Webinar on

III-V Material and HEMT Device Technology for High Power, High Frequency Applications and Modeling of LDMOS Structures

On 20th Feb, 2021

Topic: III-V material and HEMT Device Technology for High Power, High Frequency Applications

Abstract: Advancement in Si device technology has taken place due to process innovations in lithography, diffusion, ion implantation etc. Whereas advancement in III-V technology have mainly taken place due to material innovations from homo-structures to hetro-structures that paved the way for the development of new generation of devices based on confinement of carrier in quantum well with superior transport properties. Consequently III-N material based devices are being developed worldwide for high frequency, high power, broadband civil/military applications. GaN and its alloys offer many advantages compared to a III-As system, particularly a much wider range of energy bandgaps. The AlGaN/GaN hetero-junction has a large band discontinuity that can allow GaN devices to have improved output power density and improved thermal conductivity means they can operate effectively at higher temperature.The talk will mainly cover all the important aspects/challenges of GaN HEMT based device technology right from material to active/passive components, characterization and their integration to develop complete MMIC for applications up to Ku band with special focus on status of technology in India.

Dr. D. S. Rawalis an Associate Director at Solid State Physics Laboratory (SSPL), Delhi, working in the area of III-V Device Technology. He joined SSPL, Delhi in 1992 and has mainly worked for the development and Transfer of Technology of GaAs MMIC technology that is presently undergoing production at GAETEC, Hyderabad. He received his M.Sc. Degree in Physics and M.Tech. Degree in Electronics and Communication Engineering from University of Roorkee, Roorkee, India (Now IIT Roorkee), in 1988 and 1990, respectively. He did his PhD in Experimental Plasma Physics from IIT Delhi.

Presently, he is working towards the development of GaN HEMT based MMIC Technology for microwave applications. He has published more than 70 research papers in various international journals and conferences. He is also an active reviewer for various reputed international journals like Applied Surface Science (Elsevier), JVST A/B (AIP), IEEE Trans. on Electron Devuces, IEEE Sensors, Surface Coating and Technology (Elsevier), Vacuum (Elsevier), Journal of Alloy and Compounds (Elsevier), Nanotechnology (IOP science) and Journal of Physics D (IOP). He has many awards to his credit and is a recipient of DRDO Path Breaking Research Award (Twice), Scientist of the Year Award and Elsevier Outstanding Reviewer Award etc.

Topic: MODELING OF LDMOS STRUCTURES

Abstract: Lateral Double Diffused MOSFETs (LDMOS) are an important class of devices.These power MOSFETs play an important role in smart power and RF power applications. Important aspects of LDMOS structure re the breakdown voltage and on state resistance. In this talk different variations of LDMOS structures from the point of view of optimization of breakdown voltage and on-state resistance are discussed. Process and device simulations have been made on the structures. The structures such as n-channel LDMOS, stepped gate graded Lightly doped drain(LDD) structures and p-channel LDMOS structures are presented.

Speaker Profile: Dr. P. A. Govindacharyulu is presently with Manjeera Digital Systems Hyderabad as a Director. He is a Ph. D from Indian Institute of Science Bangalore. His expertise is in the areas of Semiconductor Devices, VLSI Technology, MMIC Technology and Analog and Mixed signal VLSI Design.

As the head of technology development team initially and later Head R&D. at Semiconductor Complex Ltd, Chandigarh, he was responsible for developing and implementing in production the new generation CMOS technologies which include 3-micron, 2-micron and 1.2 -micron CMOS VLSI technologies. Besides these technologies EEPROM, high voltage CMOS and CCD technologies were also implemented. After transfer to GAETEC facility at Hyderabad as Head, he was responsible for establishing the GaAs MMIC fabrication facility and implementing the 12GHz and 18 GHz MMIC technologies. MMICs were successfully developed and supplied to strategic customers like Space Department.

He was teaching VLSI related subjects such as VLSI technology, Analog and Mixed Signal IC Design etc., to ME students at Vasavi College of Engineering Hyderabad. He served as Chairman / Member on various review committees for projects sponsored by DIT (Earlier DOE), PSA's office etc., at organizations like IISc – Bangalore, IIT Bombay, CEERI – Pilani, IIT Kanpur, NIT Tiruchy, etc.

He published over 30 technical papers.Guided two students for their Ph. D in areas of device modeling and microwave circuit modeling.

Registration Details

20 February 2021 Webinar Timings: 5.30 PM to 7.30PM

Registration: Registration is mandatory for the webinar. Please register at https://forms.gle/sayyf3RSsN8FgcG77

For further details contact:

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